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RTL Verilog. In the digital circuit design, register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the data flow between hardware register, and the logical operations performed on those signals. Register-transfer-level abstraction is used in HDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived.

RTL Verilog - javatpoint

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Simulation method sacrifices performance for rich  
functionality: every active signal is calculated for  
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cycle. ... This has created a trend in RTL verification  
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the disc is white and remaining is black. When black  
portion is under sensor it generates logic 0 and logic 1  
when white portion is under sensor. Design Direction  
finder block using digital components (flip flops and  
gates) to indicate speed. Logic 0 for clockwise and  
Logic 1 for counter clockwise. Q Page 4 of 9 3/20/2006

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