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of components used in the  
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This paper presents design, implementation and comparison of highly efficient architectures for AES on FPGAs: Iterative architecture and pipelined architecture. The first design is optimized for area and the second one is optimized for speed.

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inference accuracy. An FPGA implementation is used as the validation vehicle for our design, achieving a 2.28ms inference latency for the ImageNet benchmark. Our implementation shines in

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